a multiplexer having one output line and a plurality of input lines, wherein each of said plurality of input lines is coupled to a respective one of said plurality of tap lines and said output line conveys a delayed input signal;

a phase detector coupled to said modulated input signal and said delayed input signal, said phase detector configured to produce an output pulse at an output port thereof proportional in width to a relative phase difference between said modulated input signal and said delayed input signal, said output pulse being produced in a first state when said modulated input signal leads in phase said delayed input signal and said output pulse being produced in a second state when said modulated input signal lags in phase said delayed input signal;

a charge integrator coupled to said output port of said phase detector, said charge integrator configured to produce an accumulation signal at an output terminal thereof proportional to an amount of stored charge accumulated through a plurality of output pulses received over time from said phase detector, wherein receiving said output pulse in said first state removes charge from said charge integrator by an amount proportional to said width of said output pulse and receiving said output pulse in said second state adds charge to said charge integrator by an amount proportional to said width of said output pulse;

a quantizer coupled to said charge integrator, said quantizer configured to produce a digital output signal at an output terminal thereof, wherein said digital output signal is made to change state when a level of said accumulation signal crosses a predetermined reference signal level; and

a digital integrator coupled to said digital output signal, wherein said digital integrator is coupled to said multiplexer for selectively applying a delay proportional to said state of said digital output signal to said modulated input signal to produce said delayed input signal.

10. The digital FM demodulator as recited in claim 9, wherein said quantizer is an analog-to-digital converter.

11. The digital FM demodulator as recited in claim 10, wherein said analog-to-digital converter is a one-bit analog-to-digital converter.

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12. The digital FM demodulator as recited in claim 9, wherein said quantizer is a voltage comparator.

13. The digital FM demodulator as recited in claim 9, wherein said digital integrator is a digital up/down counter.

14. The digital FM demodulator as recited in claim 9, wherein said digital integrator increases said delay if said state of said digital output signal is a logical one (1).

15. The digital FM demodulator as recited in claim 9, wherein said digital integrator decreases said delay if said state of said digital output signal is a logical zero (0).

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16. The digital FM demodulator as recited in claim 9, wherein said output port of said phase detector includes a first conductor for transmitting said output pulse in said first state and a second conductor for transmitting said output pulse in said second state.

17. The digital FM demodulator as recited in claim 9, wherein each of said quantizer and said digital integrator includes a triggering mechanism for holding an output signal level upon receiving a trigger signal applied thereto.

18. The digital FM demodulator as recited in claim 17, wherein said triggering mechanism of each of said quantizer and said digital integrator is coupled to said modulated input signal.

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19. The digital FM demodulator as recited in claim 18, wherein said triggering mechanism of each of said quantizer and said digital integrator is activated on a falling edge of said modulated input signal.